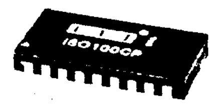
BURR-BROWN®

ISO100



Miniature
Low Drift - Wide Bandwidth
ISOLATION AMPLIFIER

FEATURES

- EASY TO USE, SIMILAR TO AN OP AMP
  $V_{OUT}/I_{IN} = R_F$, Current Input
  $V_{OUT}/V_{IN} = R_F/R_{IN}$, Voltage Input
- 100% TESTED FOR BREAKDOWN
  750V Continuous Isolation Voltage
- ULTRA-LOW LEAKAGE, 0.3μA, max, at 240V/60Hz
- WIDE BANDWIDTH, 60kHz
- LOW COST
- 18-PIN DIP PACKAGE

APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
  Transducer sensing
  (thermocouple, RTD, pressure bridges)
  4mA to 20mA loops
  Motor and SCR control
  Ground loop elimination
- BIOMEDICAL MEASUREMENTS
- TEST EQUIPMENT
- DATA ACQUISITION

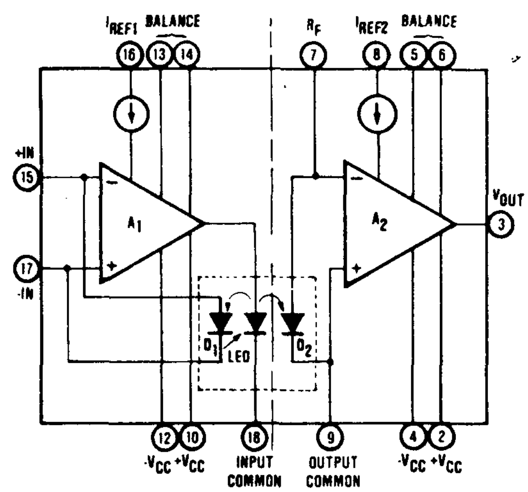
DESCRIPTION

The ISO100 is a miniature low cost optically-coupled isolation amplifier. High accuracy, linearity, and time-temperature stability are achieved by coupling light from an LED back to the input (negative feedback) as well as forward to the output. Optical components are carefully matched and the amplifier is actively laser-trimmed to assure excellent tracking and low offset errors.

The circuit acts as a current-to-voltage converter with a minimum of 750V (2500V test) between input and output terminals. It also effectively breaks the galvanic connection between input and output commons as indicated by the ultra-low 60Hz leakage current of 0.3μA at 250V. Voltage input operation is easily achieved by using one external resistor.

Versatility along with outstanding DC and AC performance provide excellent solutions to a variety of challenging isolation problems. For example, the ISO100 is capable of operating in many modes, including: noninverting (unipolar and bipolar) and inverting (unipolar and bipolar) configurations. Two precision current sources are provided to accomplish bipolar operation. Since these are not required for unipolar operation, they are available for external use (see Applications section).

Designs using the ISO100 are easily accomplished with relatively few external components. Since V_{OUT} of the ISO100 is simply $I_{IN}R_{OUT}$, gains can be changed by altering one resistor value. In addition, the ISO100 has sufficient bandwidth (DC to 60kHz) to amplify most industrial and test equipment signals.



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PDS-456E

DATA DISTRIBUTION

The SHC298 may be used to hold the output of a digital-to-analog converter whose digital inputs are multiplexed (see Figure 4).

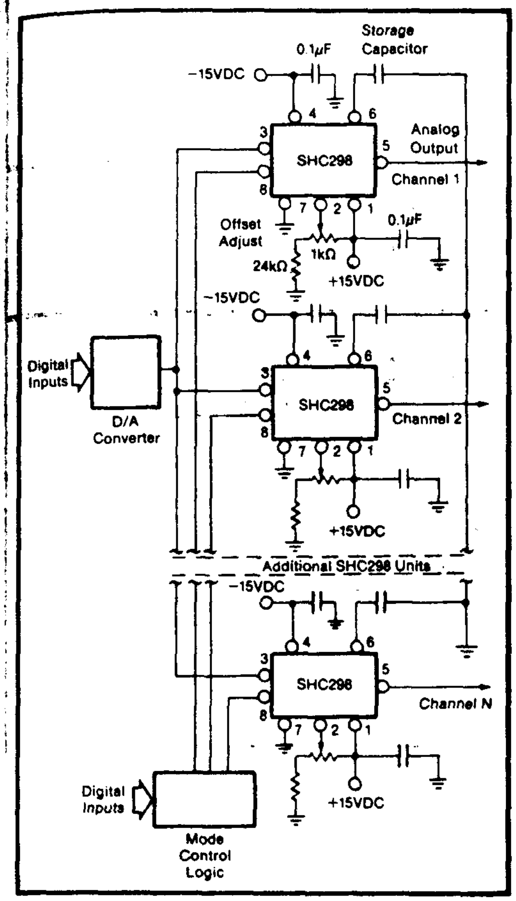


FIGURE 4. Data Distribution.

TEST SYSTEMS

The SHC298 is also well suited for use in test systems to acquire and hold data transients for human operators or for other parts of the test system such as comparators, digital voltmeters, etc.

With a 0.1μF storage capacitor, the output may be held 10 seconds with less than 0.1% error. With a 1μF storage capacitor, the output may be held more than 15 minutes with less than 1% error.

CAPACITIVE LOADING

SHC298 is sensitive to capacitive loading on the output and may oscillate. When driving long lines, a buffer should be used.

HIGH SPEED DATA ACQUISITION

The minimum sample time for one channel in a data acquisition system is usually considered to be the acquisition time of the sample/hold plus the conversion time of the analog-to-digital converter. *If two or more sample/holds are used with a high-speed multiplexer, the acquisition time of the sample/hold can be virtually eliminated.* While the first channel is in hold and switched on to the ADC, the multiplexer may be addressed to the next channel. The second sample/hold will have acquired this data by the time the conversion is complete. Then, the sample/holds reverse roles and another channel is addressed (see Figure 5) Fow low-level systems, and instrumentation amplifier and double-ended multiplexer may be connected to the sample/hold inputs. The settling time of the multiplexer, instrumentation amplifier, and sample/hold can be eliminated from the channel conversion time as before.

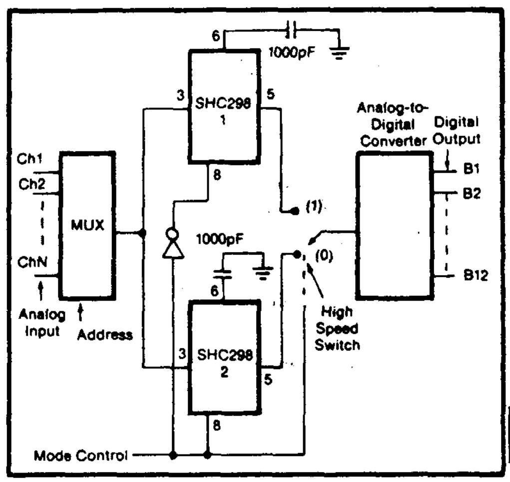


FIGURE 5. "Ping-Pong" Sample Holds.

ELECTRICAL (CONT)

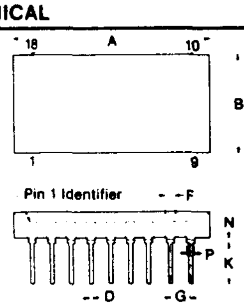
PARAMETER	CONDITIONS	ISO100AP			ISO100BP			ISO100CP			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLIES											
Input Stage											
Voltage (rated performance)			±15			•			•		V
Voltage (derated performance)		±7		±18	•		•	•		•	V
Supply Current	I_{IN} = -0.02μA		±1.1	±2		•	•		•	•	mA
	I_{IN} = -20μA		+8, -1.1	+13, -2		•	•		•	•	mA
Output Stage											
Voltage (rated performance)			±15			•			•		V
Voltage (derated performance)		±7		±18	•		•	•		•	V
Supply Current	V_O = 0		±1.1	±2		•	•		•	•	mA
Short Circuit Current Limit				±40			•			•	mA
BIPOLAR OPERATION											
GENERAL PARAMETERS											
Input Current Range											
Linear Operation		-10		+10	•		•	•		•	μA
Without Damage		-1		+1	•		•	•		•	mA
Input Impedance			0.1			•			•		Ω
Output Voltage Swing	R_L = 2kΩ, R_F = 1MΩ	-10		+10	•		•	•		•	V
Output Impedance			1200			•			•		Ω
GAIN	V_O = R_F · I_{IN}										
Initial Error (Adjustable To Zero)			2	5		1	2		1	2	% of FS
vs Temperature			0.03	0.07		0.01	0.05		0.005	0.03	%/°C
vs Time			0.05			•			•		%/kHr
Nonlinearity (3)			0.1	0.4		0.03	0.1		0.02	0.07	%
CURRENT NOISE	I_{IN} = 0.2μA										
0.01Hz to 10Hz			1.5			•			•		nA, p-p
10Hz			17			•			•		pA/$\sqrt{Hz}$
100Hz			7			•			•		pA/$\sqrt{Hz}$
1kHz			6			•			•		pA/$\sqrt{Hz}$
INPUT OFFSET CURRENT (I_{OS}, bipolar)(4)											
Initial Offset			40	200		20	70		10	35	nA
vs Temperature				3			2			1	nA/°C
vs Power Supplies				0.7			•			•	nA/V
vs Time			250			•			•		pA/kHr
POWER SUPPLIES											
Input Stage											
Voltage (rated performance)			±15			•			•		V
Voltage (derated performance)		±7		±18	•		•	•		•	V
Supply Current	I_{IN} = +10μA		+2, -1.1	+3, -2		•	•		•	•	mA
	I_{IN} = -10μA		+8, -1.1	+13, -2		•	•		•	•	mA
Output Stage											
Voltage (rated performance)			±15			•			•		V
Voltage (derated performance)		±7		±18	•		•	•		•	V
Supply Current	V_O = 0		±1.1	±2		•	•		•	•	mA
Short Circuit Current Limit				±40			•			•	mA

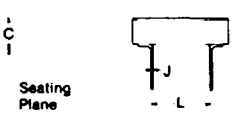
Same as ISO100AP.

NOTES

1. See Typical Performance Curves for temperature effects.
2. See Theory of Operation section for definitions. For dB see Ex. 2, CM and HV errors.
3. Nonlinearity is the peak deviation from a "best fit" straight line expressed as a percent of full scale output.
4. Bipolar offset current includes effects of reference current mismatch and unipolar offset current.

MECHANICAL





NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

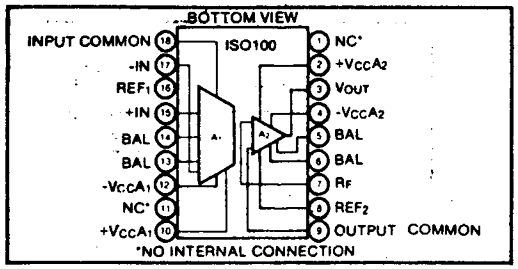
Pin numbers shown for reference only. Numbers are not marked on package.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.982	1.002	24.94	25.45
B	.480	.500	12.19	12.70
C	.148	.197	3.76	5.00
D	.016	.020	0.41	0.51
F	.050 TYP		1.27 TYP	
G	.095	.105	2.41	2.67
J	.009	.012	0.23	0.30
K	.205 TYP		5.21 TYP	
L	.290	.310	7.37	7.87
N	.015	.035	0.38	0.89
P	.040 TYP		1.02 TYP	

ABSOLUTE MAXIMUM RATINGS

Supply Voltages	±18V
Isolation Voltage	2500V
Input Current	±1mA
Storage Temperature Range	-55°C to +100°C
Lead Temperature soldering 10 seconds	+300°C
Output Short-circuit Duration	Continuous to ground

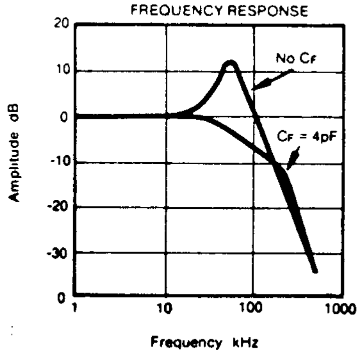
PIN CONFIGURATION



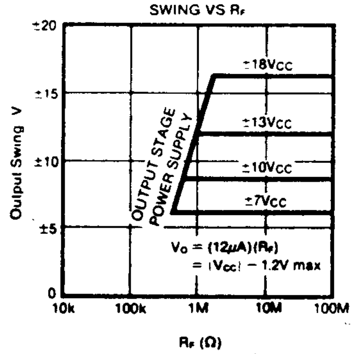
TYPICAL PERFORMANCE CURVES

T_A = +25°C, $\pm V_{CC}$ = 15VDC unless otherwise noted

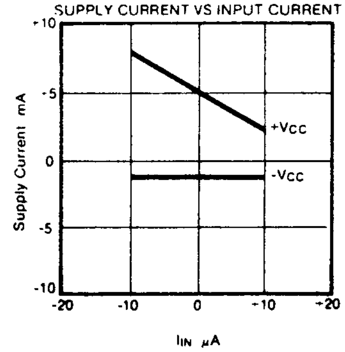
SMALL SIGNAL FREQUENCY RESPONSE



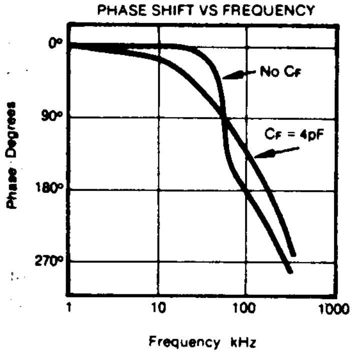
BIPOLAR OUTPUT SWING VS RF



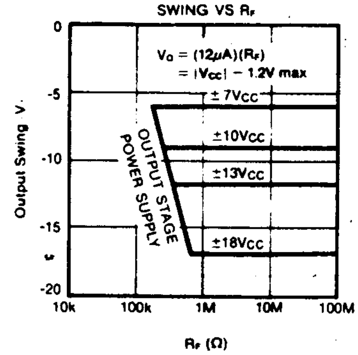
BIPOLAR INPUT STAGE SUPPLY CURRENT VS INPUT CURRENT



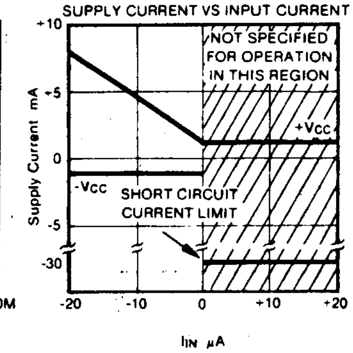
PHASE SHIFT VS FREQUENCY



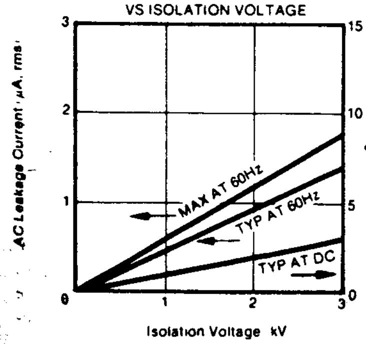
UNIPOLAR OUTPUT SWING VS RF



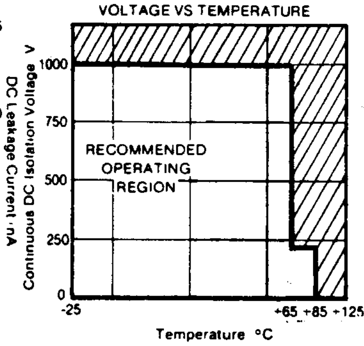
UNIPOLAR INPUT STAGE SUPPLY CURRENT VS INPUT CURRENT



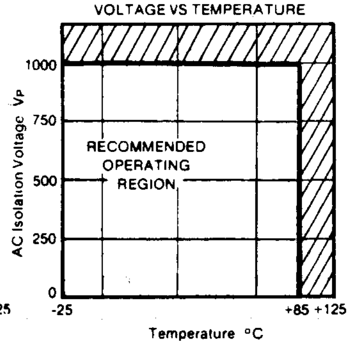
ISOLATION LEAKAGE CURRENT VS ISOLATION VOLTAGE

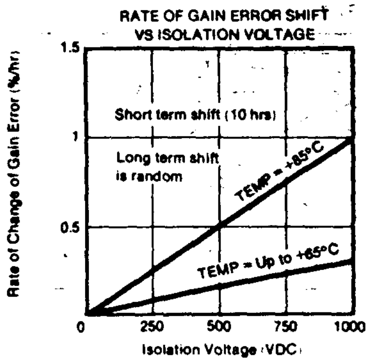


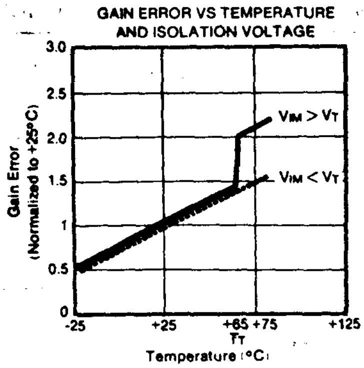
CONTINUOUS DC ISOLATION VOLTAGE VS TEMPERATURE



AC ISOLATION VOLTAGE VS TEMPERATURE







NOTES:
V_T and T_T approximate the threshold for the indicated gain shift. This is caused by the properties of the optical cavity.
T_T = +65°C, V_T = 200VDC. Shift does not occur for AC voltages.
V_{IM} = Isolation-mode Voltage
V_T = Threshold Voltage
T_T = Threshold Temperature

THEORY OF OPERATION

The ISO100 is fundamentally a unity gain current amplifier intended to transfer small signals between electrical circuits separated by high voltages or different references. In most applications an output voltage is obtained by passing the output current through the feedback resistor (R_F).

The ISO100 uses a single light emitting diode (LED) and a pair of photodiode detectors, coupled together, to isolate the output signal from the input.

Figure 1 shows a simplified diagram of the amplifier. I_{REF1} and I_{REF2} are required only for bipolar operation, to generate a midscale reference. The LED and photodiodes (D1 and D2) are arranged such that the same amount of light falls on each photodiode. Thus, the currents generated by the diodes match very closely. As a result, the transfer function depends upon optical match, rather than absolute performance. Laser-trimming of the components improves matching and enhances accuracy, while negative feedback improves linearity. Negative feedback around A1 occurs through the optical path formed by the LED and D1. The signal is transferred across the isolation barrier by the matched light path to D2.

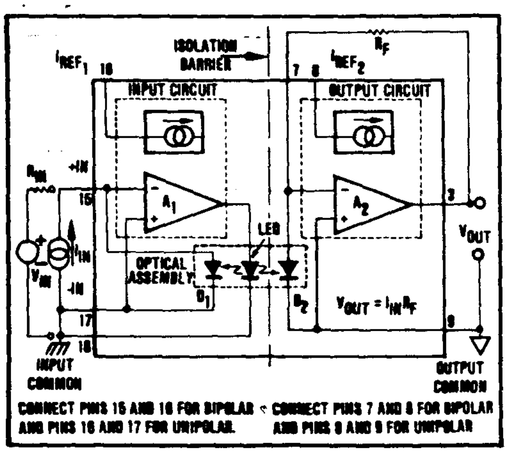


FIGURE 1. Simplified Block Diagram of the ISO100.

The overall ISO amplifier is noninverting (a positive going input produces a positive going output).

INSTALLATION AND OPERATING INSTRUCTIONS

UNIPOLAR OPERATION

In Figure 1, assume a current, I_{IN}, flows out of the ISO100 (I_{IN} must be negative in unipolar operation). This causes the voltage at pin 15 to decrease. Because the amplifier is inverting, the output of A1 increases, driving current through the LED. As the LED light output increases, D1 responds by generating an increasing current. The current increases until the sum of the currents in and out of the input node (-Input to A_1) is zero. At that point the negative feedback through D1 has stabilized the loop, and the current I_{D1} equals the input current plus the bias current. As a result no bias current flows in the source. Since D1 and D2 are matched (I_{D1} = I_{D2}), I_{IN} is replicated at the output via D2. Thus, A1 functions as a unity-gain current amplifier, and A2 is a current-to-voltage converter, as described below.

Current produced by D2 must either flow into A2 or R_F. Since A2 is designed for low bias current (≈10nA) almost all of the current flows through R_F to the output. The output voltage then becomes;

$$V_O = (I_{D2}) R_F = (I_{D1} \pm I_{OS}) R_F \approx -(-I_{IN}) R_F = I_{IN} R_F, \quad (1)$$

where, I_{OS} is the difference between A1 and A2 bias currents. For input voltage operation I_{IN} can be replaced by a voltage source (V_{IN}) and series resistor (R_{IN}) since the summing node of the op amp is essentially at ground. Thus, $I_{IN} = V_{IN}/R_{IN}$.

Unipolar operation does have some constraints, however. In this mode the input current must be negative so as to produce a positive output voltage from A1 to turn the LED on. A current more negative than 20nA is necessary to keep the LED turned on and the loop stabilized. When this condition is not met the output may be indeterminant. Many sensors generate unidirectional signals, e.g., photoconductive and photodiode devices, as well as some applications of thermocouples. However, other applications do require bipolar operation of the ISO100.

BIPOLAR OPERAT

To activate the bip
shown in Figure 1, ar
op amps. The input
unipolar operation.
has to supply all
symmetry, I_{D1} = I
matched, the curren
This results in no c
voltage will be zero
current from the inp
satisfy $I_{D1} = I_{IN} + I_{R}$
equals I_{D2}, a curren
output voltage is the
I_{IN} is limited. Positi
min). At this point,
opens. Negative I_{IN}
D1 with maximum
max).

DC ERRORS

Errors in the ISO10
voltages plus their
shown in Figure 2.

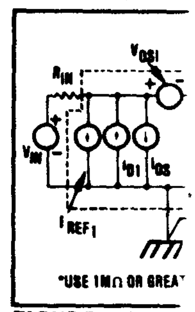


FIGURE 2. Circui

A1 and A2: ar
V_{OSO} and V_{OSI}: ar
an
ap
ap

se
I_{OS}: is
th
ze
th
o
th
m
I_{REF1} and I_{REF2}: a
c
o
m
t
I_{D1} and I_{D2}: a
d
I

BIPOLAR OPERATION

To activate the bipolar mode, reference currents as shown in Figure 1, are attached to the input nodes of the op amps. The input stage stabilizes just as it did in unipolar operation. Assuming $I_{IN} = 0$, the photodiode has to supply all the I_{REF1} current. Again, due to symmetry, $I_{D1} = I_{D2}$. Since the two references are matched, the current generated by D2 will equal I_{REF2}. This results in no current flow in R_F, and the output voltage will be zero. When I_{IN} either adds or substracts current from the input node, the current D1 will adjust to satisfy $I_{D1} = I_{IN} + I_{REF1}$. Because I_{REF1} equals I_{REF2} and I_{D1} equals I_{D2}, a current equal to I_{IN} will flow in R_F. The output voltage is then $V_O = I_{IN}R_F$. The range of allowable I_{IN} is limited. Positive I_{IN} can be as large as I_{REF1} ($10.5\mu A$, min). At this point, D1 supplies no current and the loop opens. Negative I_{IN} can be as large as that generated by D1 with maximum LED output (recommended $10\mu A$, max).

DC ERRORS

Errors in the ISO100 take the form of offset currents and voltages plus their drifts with temperature. These are shown in Figure 2.

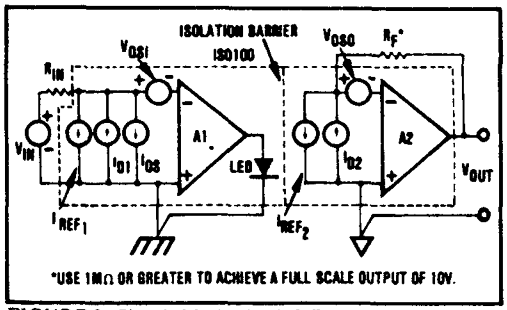


FIGURE 2. Circuit Model for DC Errors in the ISO100.

A1 and A2: are assumed to be ideal amplifiers.

V_{OSO} and V_{OSI}: are the input offset voltages of the output and input stage, respectively. V_{OSO} appears directly at the output, but, V_{OSI} appears at the output as

$$V_{OSI}\frac{R_F}{R_{IN}},$$

see equation (2).

I_{OS}: is the offset current. This is the current at the input necessary to make the output zero. It is equal to the combined effect of the difference between the bias currents of A1 and A2 and the matching errors in the optical components, in the unipolar mode.

I_{REF1} and I_{REF2}: are the reference currents that, when connected to the inputs, enable bipolar operation. The two currents are trimmed, in the bipolar mode, to minimize the $I_{OS\ bipolar}$ error.

I_{D1} and I_{D2}: are the currents generated by each photodiode in response to the light from the LED.

A_e: is the gain error.

$$A_e = |\text{Ideal gain/Actual gain}| - 1$$

The output then becomes:

$$V_{OUT} = R_F[(\frac{V_{IN} \pm V_{OSI}}{R_{IN}} - I_{REF1} \pm I_{OS})(1 + A_e) + I_{REF2}] \pm V_{OSO} \quad (2)$$

The total input referred offset voltage of the ISO100 can be simplified in the unipolar case by assuming that $A_e = 0$ and $V_{IN} = 0$:

$$V_{OUT} \approx R_F [\frac{\pm V_{OSI}}{R_{IN}} \pm I_{OS\ unipolar}] \pm V_{OSO} \quad (3)$$

This voltage is then referred back to the input by dividing by R_F/R_{IN}.

$$V_{OS\ (RTI)} = (\pm V_{OSI}) \pm R_{IN}\ (I_{OS\ unipolar}) + V_{OSO}/(R_F/R_{IN}) \quad (4)$$

Example 1: (Refer to Figure 2 and Electrical Specifications Table)

Given:
$I_{OS\ bipolar} = +35nA$
$R_{IN} = 100k\Omega$
$R_F = 1M\Omega$ (gain = 10)
$V_{OSI} = +200\mu V$
$V_{OSO} = +200\mu V$

Find: The total offset voltage error referred to the input and output when $V_{IN} = 0V$.

V_{OS} total RTI

$= \{[\pm V_{OSI} \pm R_{IN}\ (I_{OS\ bipolar}) - R_{IN}\ (I_{REF\ 1})]$
$[1 + A_e] + R_{IN}\ I_{REF\ 2}\} \pm V_{OSO}/(R_F/R_{IN})$

$= \{[+200\mu V + 100k\Omega\ (35nA) - 100k\Omega\ (12.5\mu A)]$
$[1.02] + 100k\Omega\ (12.5\mu A]\} +$
$200\mu V/(1M\Omega/100k\Omega)$

$= \{[0.2mV + 3.5mV - 1.25V]$
$[1.02] + 1.25V\} + 0.02mV$

$= -21.2mV$

V_{OS} total RTO

$= V_{OS}$ total RTI $\times R_F/R_{IN}$
$= -21.2mV \times 10$
$= -212mV$

Note: This error is dominated by $I_{OS\ bipolar}$ and the reference current times the gain error (which appears as an offset). The error for unipolar operation is much lower. The error due to offset current can be zeroed using circuits shown in Figures 6 and 7. The gain error is adjusted by trimming either R_F or R_{IN}.

COMMON-MODE AND HIGH VOLTAGE ERRORS

Figure 3 shows a model of the ISO100 that can be used to analyze common-mode and high voltage behavior.

Definitions of CMR and IMR

I_{OS} is defined as the input current required to make the ISO100's output zero. CMRR and IMRR in the ISO100 are expressed as conductances. CMRR defines the relationship between a change in the applied common-mode voltage (V_{CM}) and the change in I_{OS} required to maintain the amplifier's output at zero:

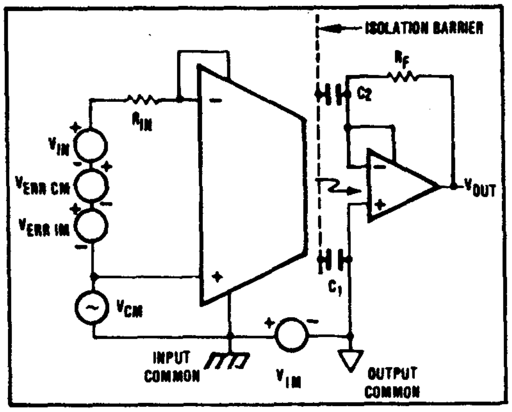


FIGURE 3. High Voltage Error Model.

$$\text{CMRR (I-mode)} = \Delta I_{OS}/\Delta V_{CM} \text{ in nA/V} \quad (5)$$

$$\text{CMRR (V-mode)} = \left[\frac{\Delta I_{OS}}{\Delta V_{CM}}\right] R_{IN} = \frac{\Delta V_{ERR\ CM}}{\Delta V_{CM}} \text{ in V/V} \quad (6)$$

IMRR defines the relationship between a change in the applied isolation mode voltage (V_{IM}) and the change in I_{OS} required to maintain the amplifier's output at zero:

$$\text{IMRR (I-mode)} = \frac{\Delta I_{OS}}{\Delta V_{IM}} \text{ in pA/V} \quad (7)$$

$$\text{IMRR (V-mode)} = \left[\frac{\Delta I_{OS}}{\Delta V_{IM}}\right] R_{IN} = \frac{\Delta V_{ERR\ IM}}{\Delta V_{IM}} \text{ in V/V} \quad (8)$$

CMRR & IMRR in V/V are a function of R_{IN}.

V_{IM} is the voltage between input common and output common.

V_{CM} is the common-mode voltage (noise that is present on both input lines, typically 60Hz).

V_{ERR} is the equivalent error signal, applied in series with the input voltage, which produces an output error identical to that produced by application of V_{CM} and V_{IM}.

CMRR and IMRR are the common-mode and isolation-mode rejection ratios, respectively.

TOTAL CAPACITANCE (C_1 and C_2) is distributed along the isolation barrier. Most of the capacitance is coupled to low impedance or noncritical nodes and affects only the leakage current. Only a small capacitance (C_2) couples to the input of the second stage, and contributes to IMRR.

Example 2: Refer to Figure 3 and Electrical Specification Table)

Given: V_{CM} = 1VAC peak at 60Hz, V_{IM} = 200VDC, CMRR = 3nA/V, IMRR = 5pA/V, R_{IN} = 100kΩ, R_F = 1MΩ (Gain = 10)

Find: The error voltage referred to the input and output when V_{IN} = 0V

$V_{ERR\ RTI} = (V_{CM})(\text{CMRR})(R_{IN}) + (V_{IM})(\text{IMRR})(R_{IN})$
$= 1\text{V}(3\text{nA/V})(100\text{k}\Omega) + 200\text{V}(5\text{pA/V})(100\text{k}\Omega)$
$= 0.3\text{mV} + 0.1\text{mV}$
$= 0.4\text{mV}$

$V_{ERR\ RTO} = V_{ERR\ RTI}(R_F/R_{IN})$
$= 0.4\text{mV}(10)$
$= 4\text{mV}$ (with DC IMRR)

(Note: This error is dominated by the CMRR term)

For purposes of comparing CMRR and IMRR directly with dB specifications, the following calculations can be performed:

CMRR in V/V = CMRR (I-mode)(R_{IN})
= 3nA/V (100k) = 0.3mV/V

CMR = 20 LOG (0.3mV/V) = -70dB at 60Hz

IMRR in V/V =
IMRR (I-mode)(R_{IN}) = 5pA/V(100kΩ) = 0.5μV/V

IMR = 20 LOG (0.5×10^{-6}V/V) = -126dB at DC

Example 3:

In Example 2, V_{IM} is an AC signal at 60Hz and

$$\text{IMRR} = \frac{400\text{pA}}{\text{V}}$$

$V_{ERR\ RTI} = V_{ERR}\ CM + V_{ERR\ IM}$
$= 0.3\text{mV} + 200\text{V}(400\text{pA/V})(100\text{k}\Omega)$
$= 8.3\text{mV}$

$V_{ERR\ RTO} = 83\text{mV}$ (with AC IMRR)

Example 4:

Given: Total error RTO from Examples 1 and 3 as 378mV worst case

Find: Percent error of +10V full scale output

$$\%\ \text{Error} = \frac{V_{ERR}\ \text{total}}{V_{FS}} \times 100 = \frac{378\text{mV}}{10\text{V}} \times 100 = 3.78\%$$

NOISE ERRORS

Noise errors in the unipolar mode are due primarily to the optical cavity. When the full 60kHz bandwidth is not needed, the output noise of the ISO100 can be limited by either a capacitor, C_F, in the feedback loop or by a low-pass filter following the output. This is shown in Figure 4. Noise in the bipolar mode is due primarily to the reference current sources, and can be reduced by the low-pass filters shown in Figure 5.

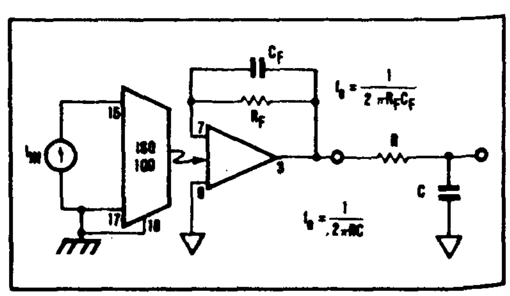


FIGURE 4. Two Circuit Techniques for Reducing Noise in the Unipolar Mode.

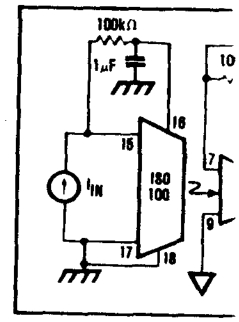


FIGURE 5. Circuit Tech
The Current

OPTIONAL ADJUSTM

There are two major sou
age and offset current.
output amplifiers can be
external potentiometers.
17. Note that V_{OSO} (500μ
output, but V_{OSI} appears
(R_F/R_{IN}). In general, V_{OS}
of I_{OS} (see Example 1).

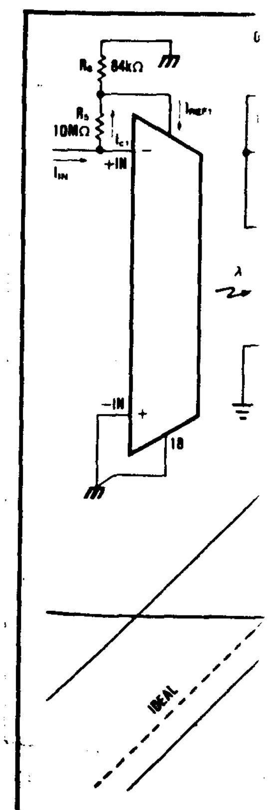


FIGURE 6. Adjusting the U
Zero Input.

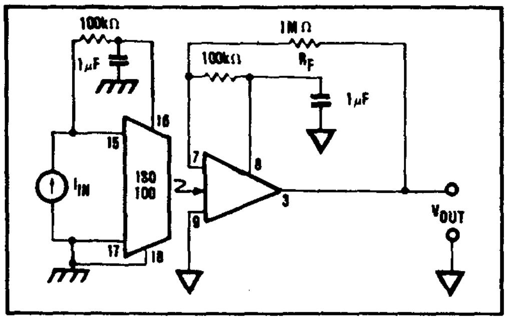


FIGURE 5. Circuit Technique for Reducing Noise from The Current Sources in the Bipolar-Mode.

OPTIONAL ADJUSTMENTS

There are two major sources of offset error: offset voltage and offset current. V_{OSI} and V_{OSO} of the input and output amplifiers can be adjusted independently using external potentiometers. An example is shown in Figure 17. Note that V_{OSO} (500μV, max) appears directly at the output, but V_{OSI} appears at the output multipled by gain (R_F/R_{IN}). In general, V_{OS} is small compared to the effect of I_{OS} (see Example 1). To adjust for I_{OS} use a circuit which intentionally unbalances the offset in one direction and then allows for adjustment back to zero.

Figure 6 shows how to adjust unipolar errors at zero input. The unipolar amplifier can be used down to zero input if it is made to be "slightly bipolar." By sampling the reference current with R_5 and R_6 the minimum current required to keep the input stage in the linear region of operation can be established. R_7 and R_8 are adjusted to cancel the offset created in the input stage. This brings the output to zero, when the input is zero. Although the amplifier can now operate down to zero input voltage, it has only a small portion of the current drain and noise that the true bipolar configuration would have.

Adjusting the bipolar errors is illustrated in Figure 7. Each of the errors are adjusted in turn. With V_{IN} = "open,", I_{OS} is trimmed by adjusting R_{10} to make the output zero. R_G is then adjusted to trim the gain error. The effects of offset voltage are removed by adjusting R_{14}.

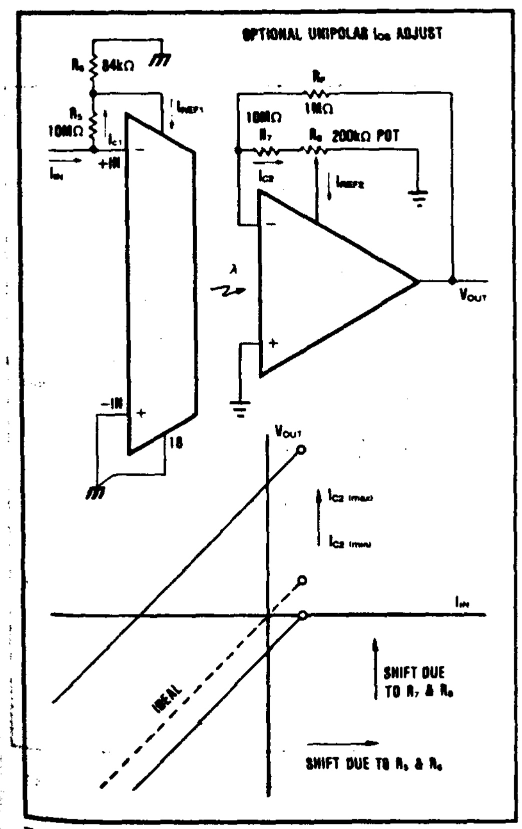


FIGURE 6. Adjusting the Unipolar Amplifier Errors at Zero Input.

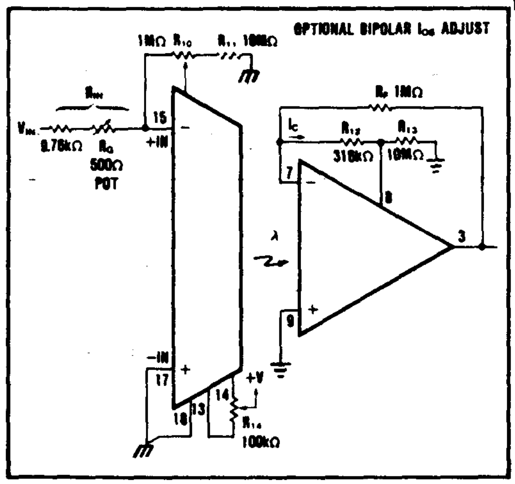


FIGURE 7. Adjusting the Bipolar Errors.

BASIC CIRCUIT CONNECTIONS

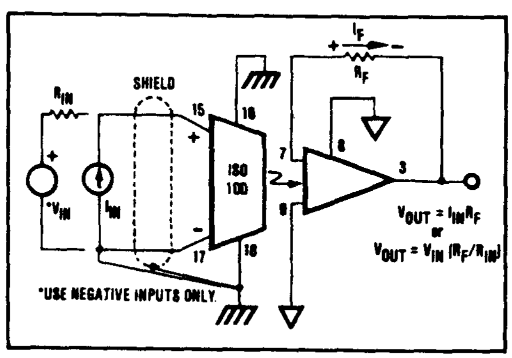


FIGURE 8. Unipolar Noninverting.

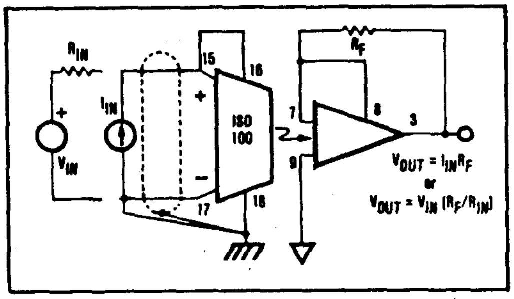


FIGURE 9. Bipolar Noninverting.

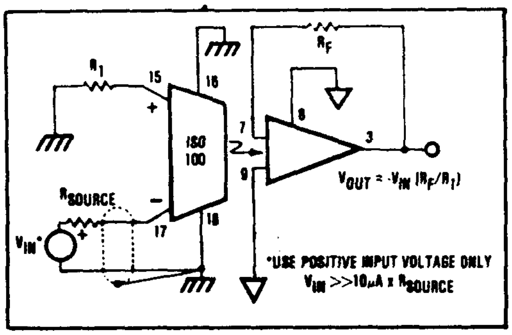


FIGURE 10. Unipolar Inverting.

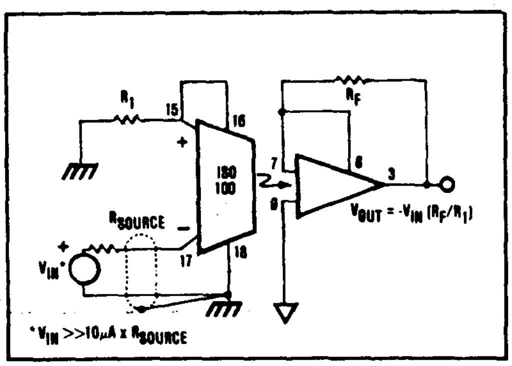


FIGURE 11. Bipolar Inverting.

APPLICATION INFORMATION

The small size, low offset and drift, wide bandwidth, ultra-low leakage, and low cost, make the ISO100 ideal for a variety of isolation applications. The basic mode of operation of the ISO100 will be determined by the type of signal and application.

Major points to consider when designing circuits with the ISO100.

1. Input Common (pin 18) and -IN (pin 17) should be grounded through separate lines. The Input Common can carry a large DC current and may cause feedback to the signal input
2. Use shielded or twisted pair cable at the input, for long lines.
3. Care should be taken to minimize external capacitance across the isolation barrier.
4. The distance across the isolation barrier, between external components, and conductor patterns, should be maximized to reduce leakage and arcing.
5. Although not an absolute requirement, the use of conformally-coated printed circuit boards is recommended.
6. When in the unipolar mode, the reference currents (pins 8 and 16) must be terminated. I_{IN} should be greater than 20nA to keep internal LED on.
7. The noise contribution of the reference currents will cause the bipolar mode to be noisier than the unipolar mode.
8. The maximum output voltage swing is determined by I_{IN} and R_F.

$$V_{SWING} = I_{IN_{max}} \times R_F$$

9. A capacitor (about 3pF) can be connected across R_1 to compensate for peaking in the frequency response. The peaking is caused by the pole generated by R_1 and the capacitance at the input of the output amplifier.

Figures 12 through 18 show applications of the ISO100.

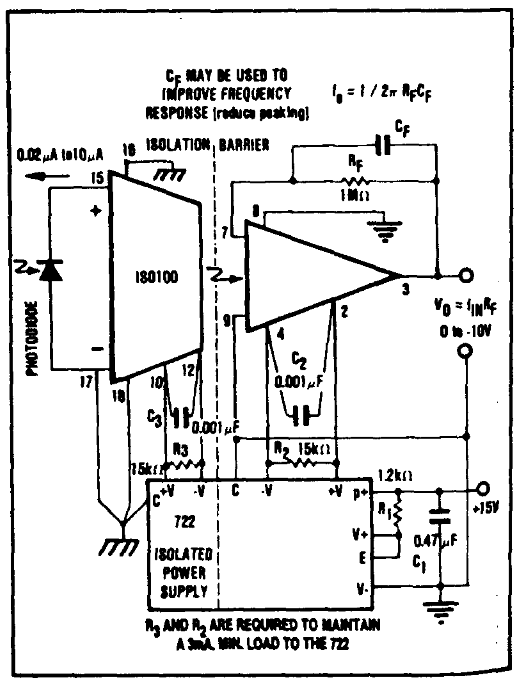


FIGURE 12. Two-Port Isolation Photodiode Amplifier Unipolar.

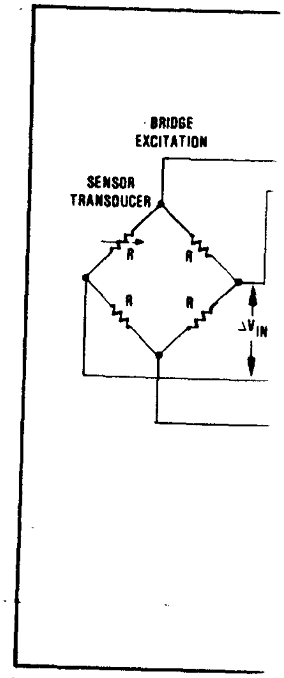


FIGURE 13. Precision Bridg

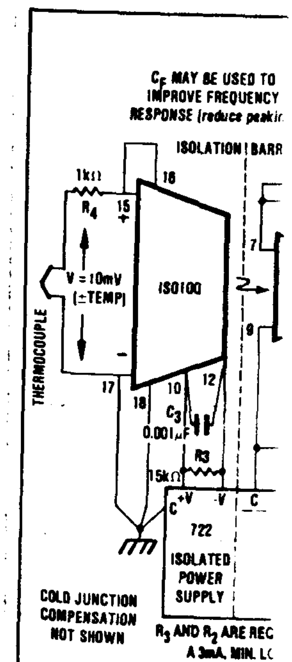


FIGURE 14. Three-Port Isol. Amplifier (Bipo

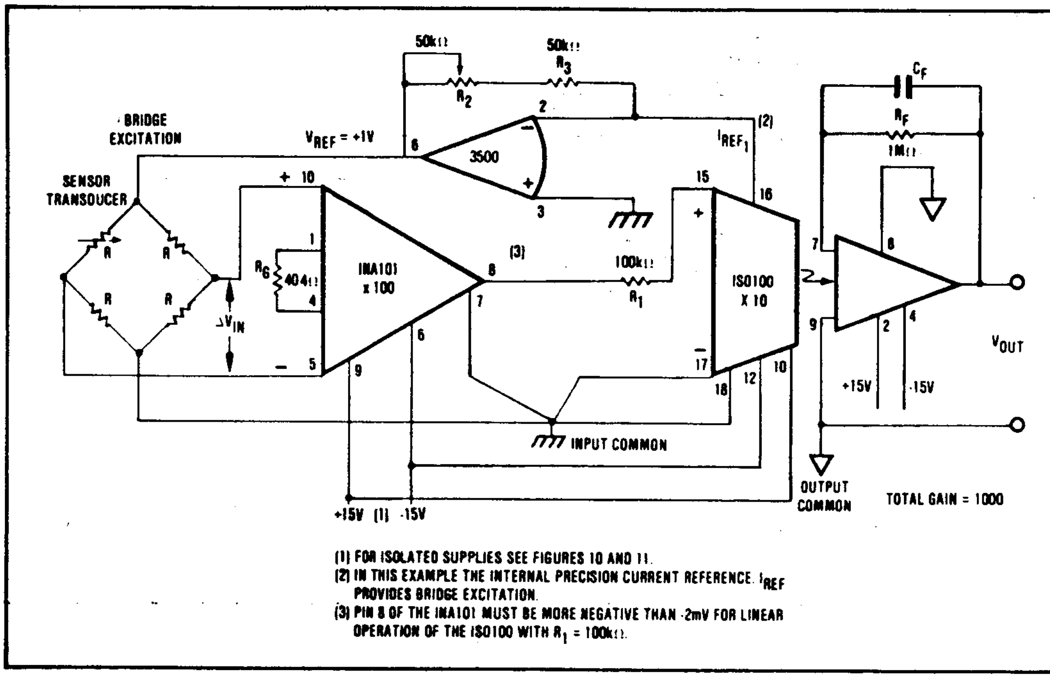


FIGURE 13. Precision Bridge Isolation Amplifier (Unipolar).

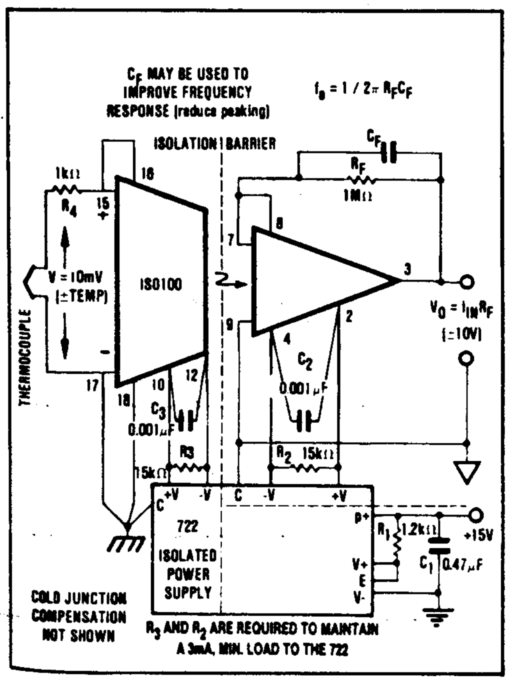


FIGURE 14. Three-Port Isolation Thermocouple Amplifier (Bipolar).

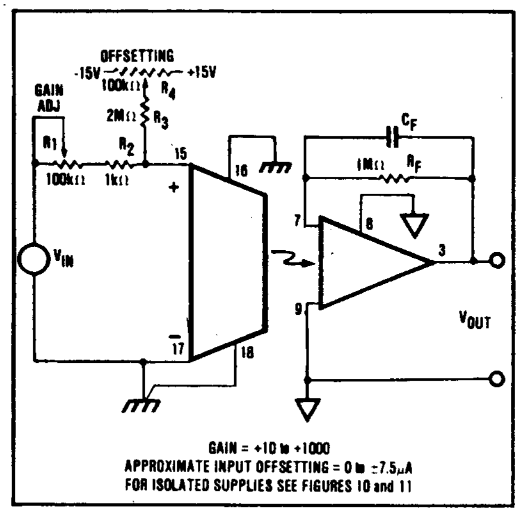


FIGURE 15. Isolated Test Equipment Amplifier (Unipolar with Offsetting).

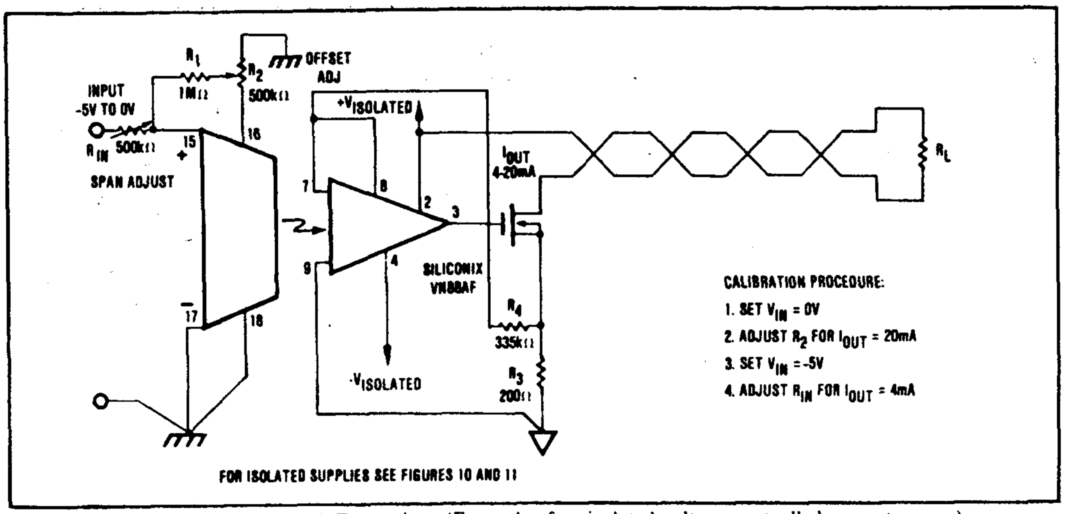


FIGURE 16. Isolated 4mA to 20mA Transmitter (Example of an isolated voltage controlled current source).

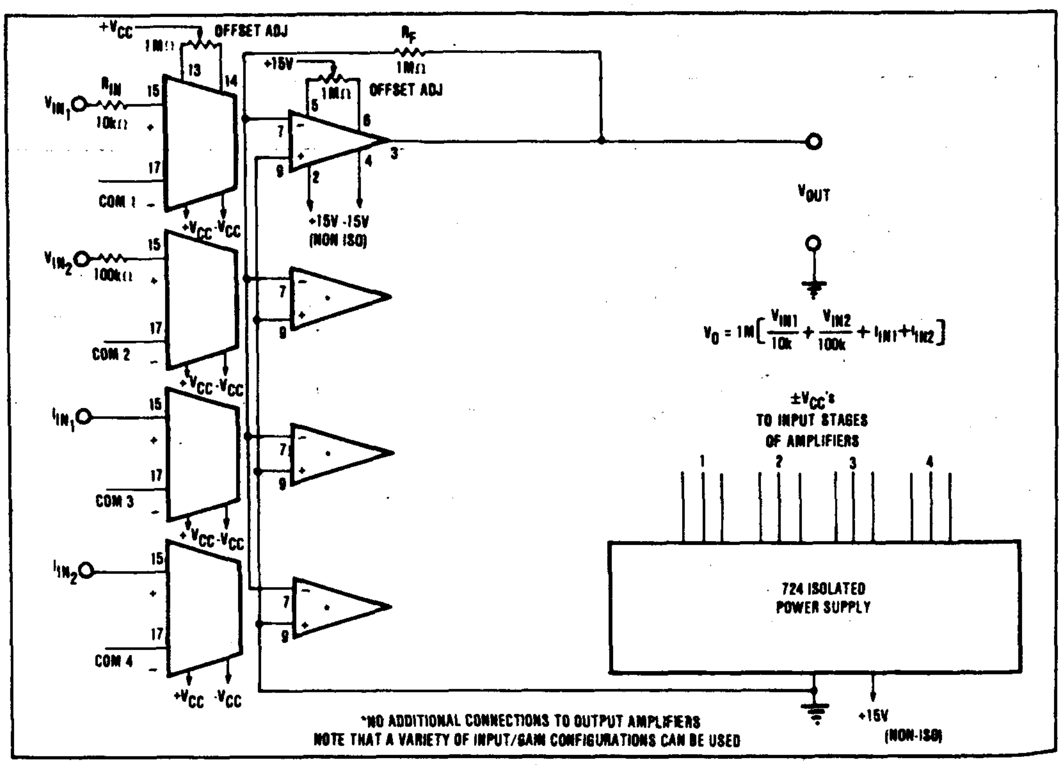


FIGURE 17. Four-Port Isolated Summing Amplifier (Unipolar).

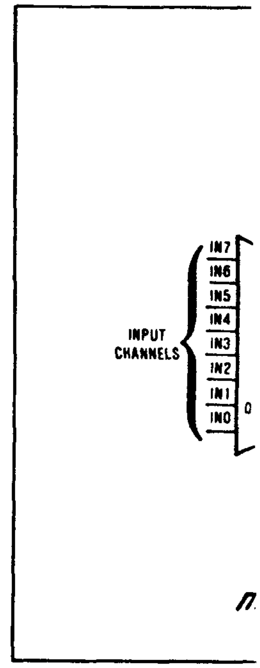


FIGURE 18. Multiple Cha
Systems).

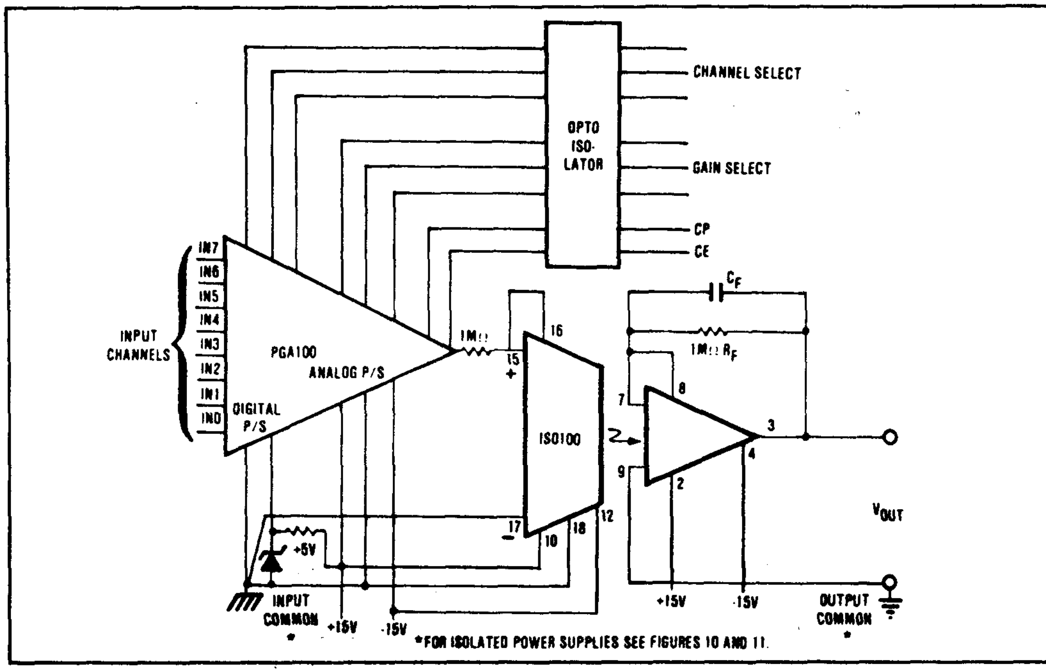


FIGURE 18. Multiple Channel Isolation Amplifier (Bipolar) with programmable Gain (Useful in Data Acquisition Systems).